Final Report

ECOSat PCB Fabrication and Component Selection

by

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Chapter 1 :

Goals:

The primary goal of this project is to process and evaluate all critical system components for the ECOSat satellite through the component selection criteria in order to minimize system failure risk, to increase reliability, and to increase robustness. Table 1 lists the critical subsystems in the satellite.

Name	Function	Predicted Hardware
Attitude Determination and Control System	Determine ECOSat's position, allowing accurate control of orientation	Sun Sensors, GPS, Magnetometers and Magnetorquer Coils
Power Regulation/ Power Generation	Regulate and Distribute power	+7V, +5V, and +3.3V voltage rails, 2 Solar Panels (14 cells)
Battery Charging	Store energy and manage pack charging and connection	16 Lithium Batteries (4s1p configuration) 2 independent boards with charge controllers
Thermal Monitoring	Maintain temperature within optimal range	Radiators for heat dissipation, Temperature Sensors for monitoring, Duty Cycle used to maintain temperature
Communications	Communicate with Control Station, Facilitate Amateur Radio	2 Dipole Antennas, 1 Digital board, 2 analog boards for up and down conversion from baseband

Table 1: Critical Systems

The secondary goal is to translate the critical system to the digital environment by performing schematic capture on each system and including the necessary peripheral documents for connecting the systems through the satellite bus, the addition of temperature monitoring to critical system, and system monitoring via the main-computer.

Once a schematic capture has been performed it must be approved and verified by design and system engineers from the ECOSat team, after this approval process the schematic is ready to be laid out on a printed circuit board. After the schematic design is translated to a printed circuit board for final implementation and design, it will be reviewed by several of the engineers on the team and undergo numerous revisions in an effort to reduce the number of post-production revisions.

The end goal is to have all the critical systems designed and laid out on printed circuit boards ready for final assembly in a class 10,000 clean room.

Chapter 2 :

Project Overview

Our team, has approved and verified 157 discrete components (resistors, capacitors, inductors, integrated circuits, connectors, and wires) for various subsystems, performed schematic capture on four of the five critical systems, and designed three of the five printed circuit boards for the UVic ECOSat team.

The currently designed printed circuit boards consist of the Power Regulation/Power Generation, Battery Charging, Thermal Monitoring, and Communications systems. The Attitude Determination and Control System is slated for design next and will continue on past the end of this project class.

Power System:

ECOSat's power system requirements consist of three voltage rails at 7V, 5V, and 3.3V having ampacities of 2.3A, 1.5A, and 1A respectively. Two solar panels, each consisting of 7 cells in series, will provide a nominal voltage of 17.5V and a peak power of 7 Watts per panel.

Battery System:

The battery charging and storage system consists of sixteen lithium-ion battery cells that will store excess energy generated from the two solar panels and will discharge when the satellite power demands exceed the power generated by the solar panels.

The battery cells are configured in a 4s1p (4 in series, 1 in parallel) configuration with two packs attached to a single printed circuit board, a charge controller for the battery packs is also integrated into the design as well as temperature monitoring for each cell. Two such printed circuit boards will be included in the system stack in order to have a fully redundant backup for both charging circuitry and energy storage.

Thermal Monitoring:

Thermal monitoring for the satellite consists of two sets of digital temperature sensors sourced from Analog Devices Inc, a generic template for the sensors has been created and is included in all critical systems for ensuring that devices remain in their safe operating area.

Communication System:

The communication system is currently under design revision by another project team, although part selection and approval is ultimately the final responsibility of this team.

Templates:

In an effort to reduce design time templates have been created for any document that will be included in multiple systems in order to not only increase efficiencies but to guarantee a consistent quality of work. This includes not only schematic templates, and project templates, but a printed circuit board template to ensure that all boards are designed with the correct mechanical specifications for both the standoff connections, and system bus, as well as the mechanical size constraint of the boards.

ECOSat and their sponsors provide all the components required for finalized system designs.

Chapter 3 :

Detailed Project Description

The University of Victoria's Experimental Cosmic Ray and Diamagnetic Scientific Satellite (ECOSat) is designing and building a nano-satellite that is less than 4kg and conforms to 10cmX10cmX33cm (Cubesat) for entry into the Canadian Satellite Design Challenge. The ECOSat team is then further divided into sub teams for each subsystem Communication, Power, Attitude Determination and Control System, Main Computer, Solar Panels. Each of these sub-systems will have further task breakdown and have a team leader that oversees work flow and distribution.

The focus of the competition is to research, design, and build a fully functional Cubesat that will be capable of carrying out the chosen mission of the ECOSat team. The Cubesat will be subjected to complete environmental testing as well as a pre and post flight system check to confirm the satellite operability after a simulated launch procedure.

One of the critical aspects that for the team that required in depth research was the design and fabrication of the printed circuit boards for space applications.

Design Method Used

The Satellite has been designed from the outside in using a divergence design method, by exploring possibilities and constraints of the problem, then through qualitative and quantitative research methods to develop better understanding toward better design solutions. By using the competition specified dimensions of the satellite structure, the internal sub systems have been modeled and designed to conform the specified form factor, through the use of solid modeling techniques and prototyping.

Due to the competition requirements, the driving factors for the satellite design are the form factor 10cmX10cmX33cm and a mass not exceeding 4kg. Additional factors influencing the satellite design are the requirements to have total off-gassing less than

.3% by mass, surviving launch conditions both depressurization to vacuum and 12G accelerations in all axes.

Relevant Information

The competition is designed to use commercial of the shelf (COTS) components for the designs; however there are still several parameters which must be taken into account when considering component selection.

The primary issue which has arisen is the growth of tin whiskers, from tinned component leads. Tin whiskers are electrically conductive, crystalline structures of tin that sometimes grow from surfaces where tin (especially electroplated tin) is used as a final finish. Tin whiskers have been observed to grow to lengths of several millimeters (mm) and in rare instances to lengths in excess of 10 mm.

Numerous electronic system failures have been attributed to short circuits caused by tin whiskers that bridge closely-spaced circuit elements maintained at different electrical potentials. This is the primary concern for the electronic circuits aboard the satellite due to the high component density of the circuits.

The mechanism for which causes the tin whisker growth is still unknown. Some theories suggest that tin whiskers may grow in response to compressive stress relief within the tin plating. This theory helps to support the fact that increased growth of tin whiskers is observed when in vacuum.

Other factors influencing the circuit designs are selection of component construction material and dielectric properties for Capacitors, Inductors, and Resistors. The radiation background noise that the devices and boards will be subjected too also plays a significant role in the design and optimization of the printed circuits.

Design Choices

Avoiding the use of pure Tin plated components is the best option, however if this proves impossible due to part availability or other design trade-offs with comparable components. It is also impractical to rely on manufacturer's certification that pure tin plating was not used in the production of the product supplied. NASA has several documented cases where the procurement documentation specified "no Pure Tin" but was later determined to be pure tin.

Methods for preventing tin whisker growth is Solder Dipping the plated surfaces in order to completely reflow and alloy the tin plating. Re-plating the affected area using a suitable plating alternative such as (Sn-PB, CU, AG etc…) on top of the existing pure tin deposit will prevent the growth of whiskers. Silicone conformal coating or foam encapsulation is also a recognized prevention method in order to significantly reduce the risk of electrical shorts caused by whiskers.

Final Design

The final design of the satellite will be complete by September 2012; currently the selected components for the satellite conform to the aforementioned selection criteria. Additional manufacturing techniques for the printed circuit board (PCB) substrates have been selected in order to prevent tin whisker growth, the PCB manufacturer offers these services as part of our sponsorship they are a Military and Aerospace certified manufacturer of PCBs.

The first systems that will have PCB's manufactured for the flight model will be the Communications systems, and the Power management system consisting of 3 switch mode power supplies at 15V, 5V, and 3.3V, as well as a Maximum Power Point Tracker for the solar cells, and a Battery Charging system for the Lithium-Ion Cells.

Chapter 4 :

Workload Distribution:

Justin Curran:

Component verification and final approval, responsible for the generation of template files for use in schematic capture and printed circuit board design. Additional responsibilities include the design and layout of the power regulation system, Attitude determination and control system, and Battery charging system. Additional duties during the project include the generation of documentation for ELE 399 including book reviews and website design.

Robin Novlesky:

Responsible for assisting in component verification, generation of communication protocol documents for distribution throughout team structure and for architecting the overall bus design. Additional responsibilities include assisting in the design and layout of the, Attitude determination and control system, and Battery charging system and full generation of the Digital communication printed circuit board.

Gorkem Cipili:

Responsible for software design for the communication system including protocol and modulation techniques.

Nigel Syrotuck:

Responsible for team management, outreach activities, and mechanical structure

Kris Dolberg:

Responsible for magnetorquer circuitry design, construction, and testing.

Dan Kennedy:

Responsible for environmental testing, and main computer software architecture

Justin Sakarookoff:

Responsible for sensor integration with the attitude determination and control system, including GPS

Chapter 5 :

Project Discussion

From the time of the previous report there has been much development in a number of systems and subsystems, each system will be identified and discussed separately.

A PCB template has been developed for all system boards that will be housed in the PCB stack. This has been done to ensure the proper alignment of the stack connector and standoffs for all PCBs in the system stack. Additional parameters and special strings have been added to the PCB template in order to automatically generate manufacturing documentation upon creation of the artwork files; this additional information consists of a layer stack up legend, drill legend, and layer names.

Attitude Determination and Control System (ADCS):

The ADCS system and its sub-systems GPS receiver, Sun Sensors, Magnetometer, and Magnetorquers have undergone much development and revision in the past weeks. The Magnetorquer, Magnetometer, and Sun Sensor systems will be discussed as they have undergone the component selection criteria and have begun to be laid-out and designed on printed circuit boards.

ADCS Main PCB:

The GPS adapter board is currently under development in order to connect the 20 pin general purpose input/output port of the GPS receiver to the ADCS main PCB which hosts the micro-controller for the system and the magnetometers, as well as the connection ports for Magnetorquer drive circuit and the Sun Sensors.

The magnetometers selected is a single chip solution for measuring three axes x,y,z from Freescale Semiconductors. The selection criterion for this chip was based on its resolution, communication interface, and small form factor, the sensor datasheet specifies that the leads for the chip are not pure tin.

Since the Sunsensor(s) and Magnetorquer(s) sub systems will have their own standalone PCBs the systems will connect to the main ADCS board through the system bus stack and wiring harness.

The Sunsensor(s) will have dedicated thick film current sense resistors connected to an automotive grade 24-bit delta-sigma ADC that will provide a digital readout to the ADCS micro-controller.

Similar to the Sunsensors the Magnetorquer board will be remote from the ADCS main PCB. The Magnetorquer PCB will have the three torque coils as well as the drive circuitry for the system integrated into a single board with components for the drive system laid out on both sides of the PCB in order to reduce magnetic interference between the electronics on the board and the Magnetorquer coils. A special low off gassing enamel aluminum wire has been selected for the windings of the Magnetorquers.

The ADCS system is scheduled to be designed in the coming week.

Battery System:

The battery charging system for the satellite implements a Linear Technology charge controller the LTC1960, the controller features SPI communication for the management of cell charging and pack connection to the battery bus, it is capable of managing two independent battery packs. The batteries selected for the system are Panasonic UR14650 Lithium Ion cells, which come from the same Panasonic chemistry line as cells which have a long flight heritage in the aerospace industry. The cells were additionally chosen for their wide temperature operating range, high energy density, low mass, and small form factor. Product availability and cell mounting configuration (welded tabs) also played a strong factor in the selection of this particular cell.

One such charge controller will be used to manage the charging of each battery pack, of which there will be two per printed circuit board. In this manner it will always be possible to have at a minimum of one battery pack connected to the bus in order to help suppress voltage fluctuations. In addition there will be two such printed circuit boards in the satellite design there by making the system double redundant for the charge controllers and the battery packs have the added feature of being quad redundant. **Figure**

1: Battery PCB below depicts the layout for the battery board; it is currently missing the charge controller integrated circuit, it should be noted that there are cells on both sides of the printed circuit board.

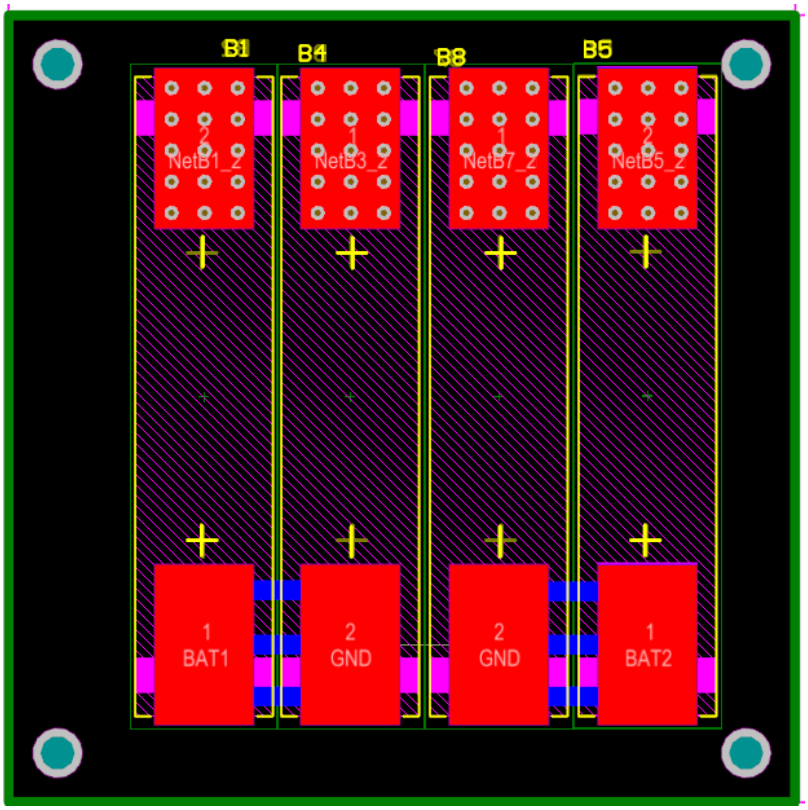

Figure 1: Battery PCB

Communication System:

The communication system has two analog PCBs under development an analog transmitter and receiver. The boards have undergone several rounds of redesign in order to refine the system in an effort to reduce post prototype design revisions. Many of the board changes have been due to manufacturing constraints for the PCB, in particular minimum feature size of footprints, silkscreens, and finished hole sizes for the Vias.

Also to reduce the costs of manufacturing the number of different hole sizes has been reduced from seven separate drills to four which greatly increases the manufacturability of the design as well as reduce costs. Preliminary testing and final design revisions are currently being conducted on the system.

Power System:

The switch mode power supply for the power regulation board is one of the more difficult designs for part selection since each regulator has several dozen parts many of which are large capacitance values that require low ESR and high ripple current filtering. To help simplify the approval process the integrated circuits for the 7v, 5v, and 3.3v system all use the same family of devices and therefore also use very similar components in their design, there by simplifying the overall part approval process.

Additionally the output inductors for each regulator require a large footprint area. In order to optimize area without sacrificing performance the problem arises that there is a direct trade-off between ripple current filtering (filtering performance) based on the inductance value and the power dissipation (thermal performance) in the inductor. The currently chosen inductors are the best trade off between power dissipation, ripple filtering, and printed circuit board area.

The current PCB for the system has been designed around using automotive grade components to reduce thermal risk; additionally all electrolytic capacitors have been replaced by sealed tantalum capacitors for their greater temperature stability, improved high frequency filtering and linearity. The inductors have also been chosen carefully from Coilcraft for their high shielding and low off-gassing properties.

The switch mode power controllers have all been chosen from the National Semiconductor line of Automotive Grade 0 integrated circuits. The printed circuit board depicted in **Figure 2: Power Regulation PCB** shows the current state of development for the power regulation system.

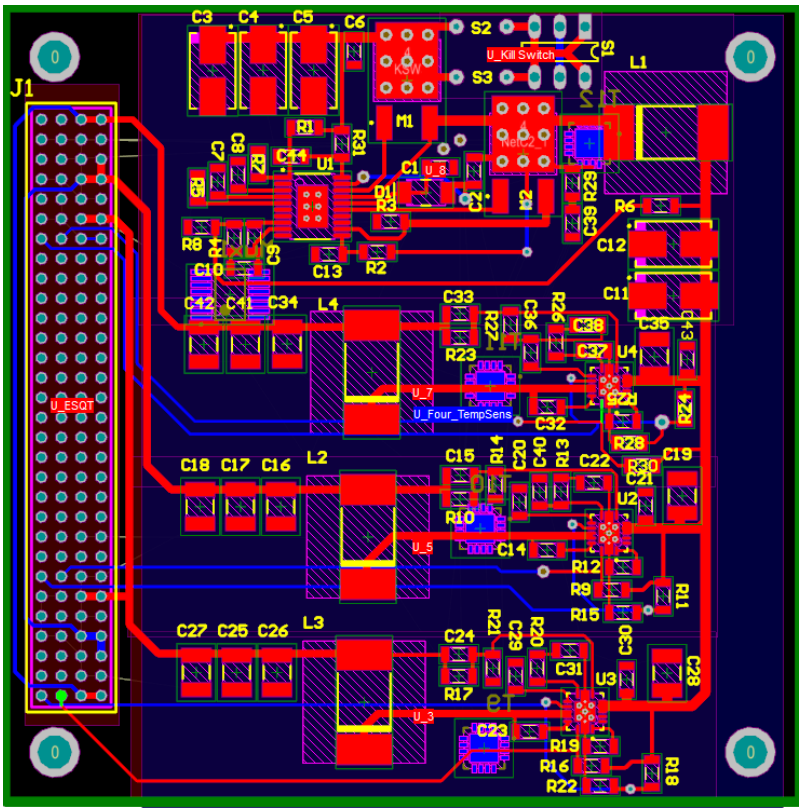

Figure 2: Power Regulation PCB

Thermal Monitoring:

Two sensors from Analog Devices Inc have been selected for the final design implementation. The sensors were chosen for their rich feature set (over and under temperature interrupts), wide temperature sensing range -55C to +150C, high linearity, self-calibration, low junction to case thermal impedance, and their communication protocol for interfacing with the main computer.

Two sensors were implemented for the final design due to the limited availability of one sensor the ADT7320 is currently only available as a pre-release sample. The ADT7320 is preferred over the ADT7310 solely for its reduced thermal impedance 7°C/W vs 37°C/W and minimal footprint areas, apart from these parameters the sensors are identical. The schematic depicted in **Figure 3: Temperature Sensor Schematic** below shows the file that is included with the critical systems for the incorporation of temperature monitoring.

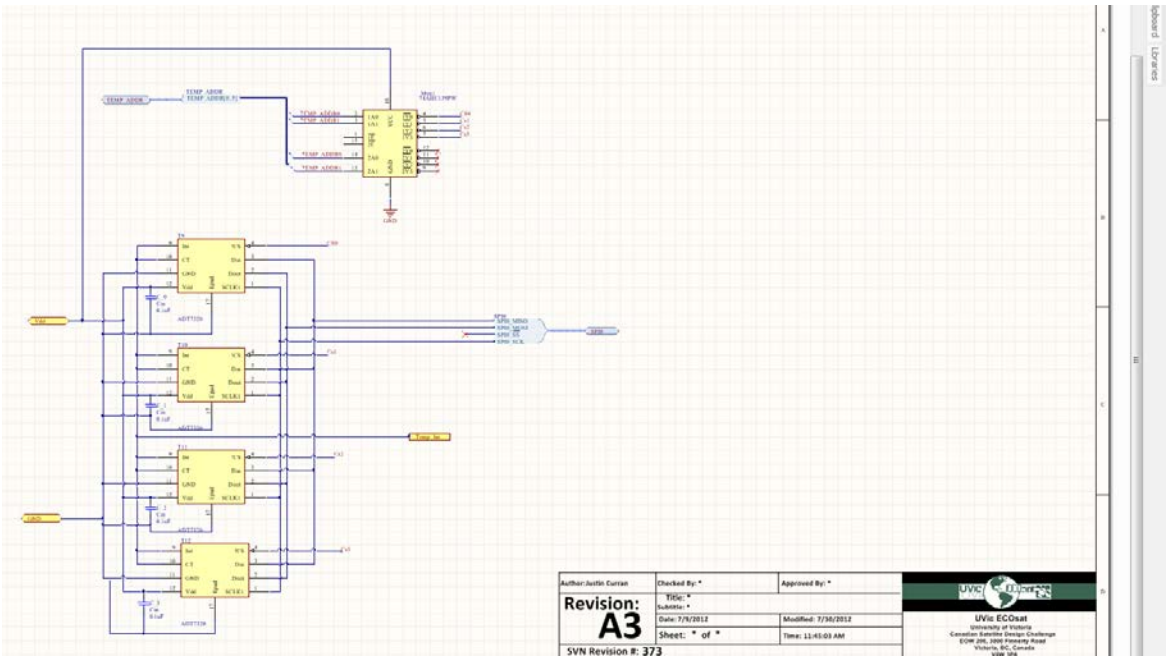

Figure 3: Temperature Sensor Schematic

Templates:

Several templates have been created for both schematic capturing and printed circuit board design. A depiction of the system bus template can be seen below in **Figure 4: Bus Schematic Template** this is the reference document for inclusion in all systems that will be connected to the system stack bus.

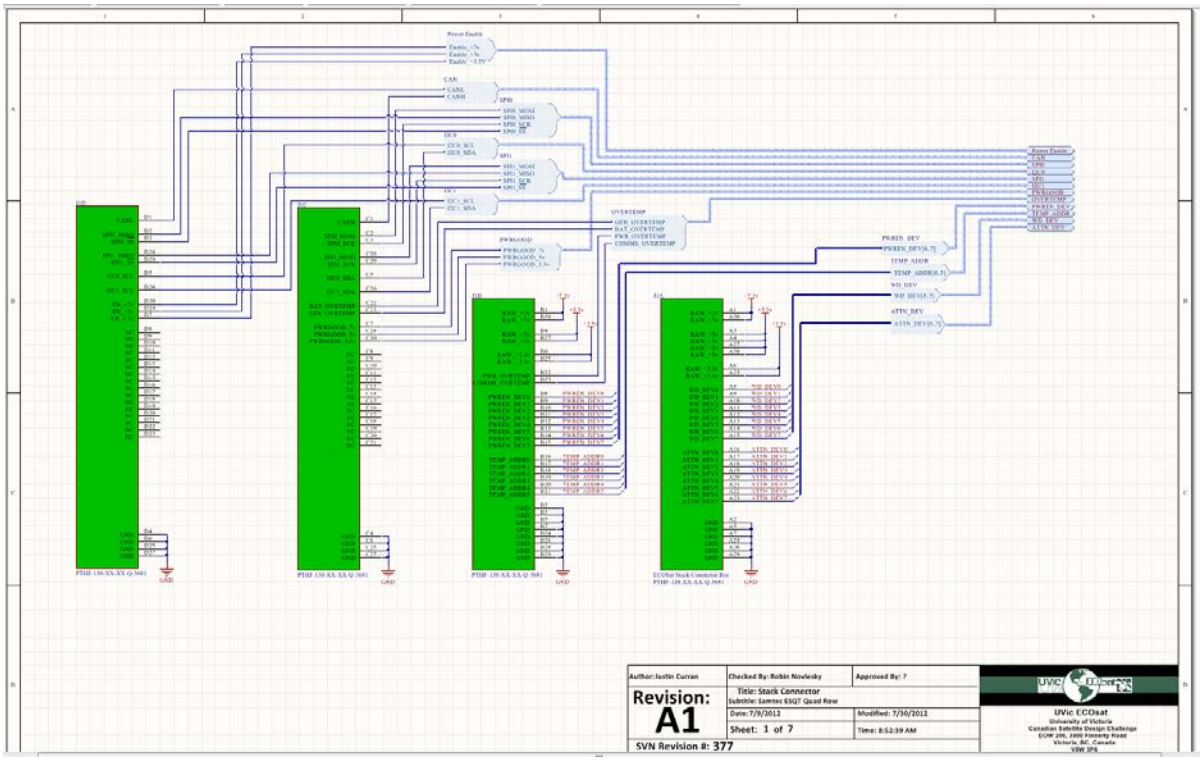

Figure 4: Bus Schematic Template

The creation of a printed circuit board template ensures that for the final design all standoff locations will conform to a single set of coordinates as well as the boards will have the same overall mechanical tolerances. It can be seen in the depiction below **Figure 5: PCB Template** that the template consists of a board outline, standoff location, mechanical dimensions, as well as special strings for artwork generation during fabrication (layer stack up, drill legend, and layer names).

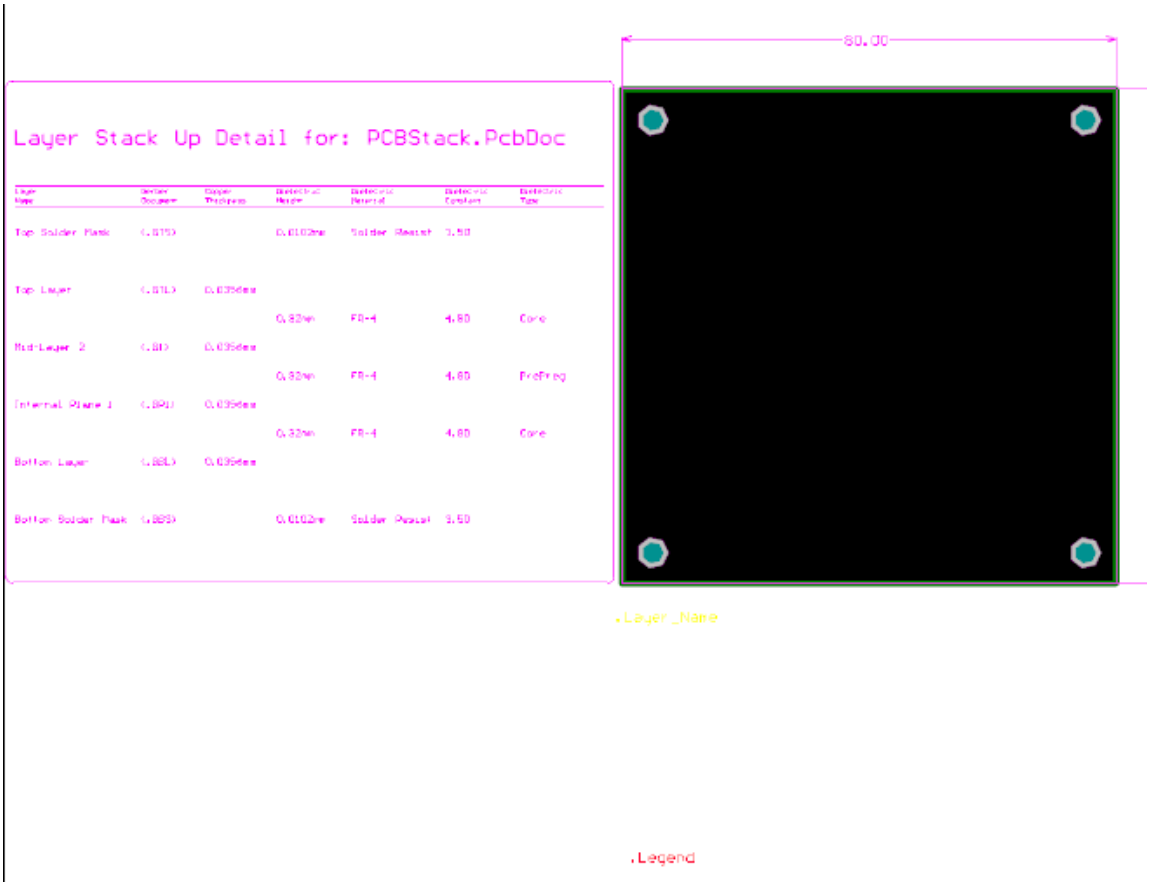

Figure 5: PCB Template

The drill legend and layer name are compiled only when the artwork files are generated, during normal viewing in the PCB editor it shows the special string names.

Chapter 6 :

Summary:

The project has made much progress and overcome a number of obstacles, however currently the project is behind schedule based on the Gantt chart projections however many of the previously anticipated project holdups and difficulties in procuring certain components for subsystems have been resolved. The remaining issues to be resolved can only be taken care of during the design qualification phase in order to guarantee the systems operating parameters and performance criteria.

Designs are actively being reviewed by the author and team members as well as working professional RF and Design engineers currently no critical errors have been found and prototyping is continuing un hindered. However workloads from outside sources and other academic classes are threatening the progress of the project and could potentially threaten the overall feasibility of the project.

Future Works:

There is much work to be conducted between now and the end of September, work will continue unabated past the completion of the ELEC 399 class curriculum. The power systems PCB will be finalized next with the addition of a few minor components, and then battery charging system will be next in the design verification plan, followed by the ADCS and main CPU. The communication boards will be designed in parallel by another team of engineers.

Appendix A: Textbook Review/Synthesis

Chapter 12:

In the construction phase the first duty is to break up the work and assign it to team members, this is hopefully done with a minimal amount of people in order to reduce complexity in coordination of team members. As the team grows in numbers it becomes more difficult to have a synergistic team that is transparent with its action. Some of the coordination can be assisted or improved via the use of software such server side file revisioning, in addition to weekly meetings, and other computer aided software tools.

Typically at this stage in project development the most common delays are scope creep and slippages that go unnoticed this all tends to add up and push back deadlines and ultimately puts the project off the schedule laid out by the Gantt chart.

At the construction phase, test planning is also a crucial step, not only the execution of testing but the design of tests in order to have full fault coverage. Fixing problems and bugs that were missed by testing after the installation of a system is not only costly by a monetary stand point but also by a time metric as it can take much longer to fix or resolve issues once a system is implemented.

At this stage it is also crucial that proper documentation is generated in order to for the system to be well understood and easily troubleshot or modified in future revisions. The documentation consists not only of system documentation but user documentation for the instruction of its operation and function. There are typically three types of documentation reference documentation, procedure manuals and tutorials.

Chapter 13:

When introducing new systems or technology a transitioning period must be undertaken to familiarize users and aid them in the transition, the typical model used for this is Lewin's three step model of organizational change, unfreeze, move, and refreeze. This is typically done in an effort to move users from the as-is system to the to-be system. Good support and proper documentation will help to refreeze the users with the new system.

The migration plan encompasses all aspects of the project not simply the transitioning of the employees, but the installation and verification of the system, in addition to the overall culture of the organization. A well-developed migration plan will help to identify sources of resistance during the migration process and aid in the resolution of the resistance in order to increases the users' perceived benefit of the transition and aid in the users buying in to the new system.

When addressing system support a two tier response system is typically employed the first tier interacts directly with users and provides support, while the second tier tackles more challenging problems that cannot easily be resolved possible bug correction, or system implementation. Additionally the system could also require maintenance either due to regular use or resulting from change orders submitted from the user population. At this stage the project is typically assessed for its effectiveness both in its implementation and in the project activities, additionally this would highlight what needs to be improved for future projects and what was done correctly and should be continued.

Chapter 14:

The biggest change in today's environment is the migration to object orientated techniques which views systems as a whole with action items and data contained in a single element. This is not a new concept but is one that has gained footing and has become prevalent in the software programming environment.

This concept can be extended to object orientated analysis for systems to allow an analyst to decompose complex problems into smaller, easily managed components through a commonly accepted notation format called UML. UML is a standard set of diagramming techniques and procedures to easily represent any system element as a graphical symbol; this is typically done from analysis to implementation phases.

Chapter 7 References

1. Space Mission Analysis and Design 3rd ed , James R. Wertz & Wiley J. Larson
2. Spacecraft Attitude Dynamics, Peter C. Hughes
3. System Analysis and Design 4th ed , Alan Dennis, Barbara Haley Wixom, Roberta M. Roth
4. Spacecraft Systems Engineering 4th ed. - P. Fortescue

ELEC/CENG 399 Design Project I

Progress Report II Evaluation Form

To be filled by students:

Project title: ECOSat PCB Fabrication and Component Selection _____

Group #:_____

Group members: Justin Curran

Supervisor(s): Dr. Peter Driessen

To be filled by the supervisor(s):		
Progress report distributed to the supervisors for grading: Friday, August 3, 2012		
Please complete the progress report grading by: **Friday, August 17, 2012**		
Please refer to the rubric for grading.		
Topics		Grade [%]
[5%]Chapter 1, Goals :		
[10%]Chapter 2, Progress Overview:		
[25%]Chapter 3, Detailed Project Description:		
[25%]Chapter 4, Workload Distribution and Achievements:		
[10%]Chapter 5, Project Discussion:		
[5%]Chapter 6, Summary and Future Works:		
Subtotal [80%]:		**0.0**
To be filled by the instructor:		
[20%]Appendix A: Textbook Review	[10%]Write the textbook review in a clear	
	[10%]Meet minimum page requirement (2 pages):	
	Subtotal [20%]:	**0.0**
Total [100%]:		**0.0**

Chapter 8 Comments by the supervisor: